AMENDMENTS TO THE SPECIFICATION:

Page 1, amend paragraph [0001] as:

[0001] The present invention relates to power feedback power factor correction high frequency ~~inverter~~ inverters, and more particularly to the [[to]] power feedback power factor correction high frequency inverter used for a lamp ballast.

Page 1, amend paragraph [0002] as:

[0002] Electronic lamp ~~ballast~~ ballasts currently available on market~~, having~~ have a circuit as shown in Figure 1, which comprises an AC (alternate current) filter circuit 10, a bridge rectifier circuit 11, a DC (direct current) rectifier circuit 12 and a DC/AC conversion circuit 13. The electronic lamp ballast drives a lamp tube 14 to start irradiating. However, the DC rectifier circuit 12 of the known electronic ballast uses only a single capacitor 20 to form the filter circuit. ~~Though~~ Although it has the advantages of low cost, simple circuit, and high load variation resistance, yet this type of filter circuit has a shorter period of charging current[[,]] which occurs only when the voltage at the power source side is higher than the voltage drop across the capacitor at its DC output side. Therefore, the known circuit produces a large ripple current and, consequently, ~~leading~~ leads to low efficiency. As such, the power factor of the known ballast is merely between 0.5 and 0.6 as shown in Figure 2, which shows, for the known device, the input ripple current is large and the power factor is low. This phenomenon apparently leads to the result of increasing power consumption and the waste of power.

Page 2, amend paragraph [0005] as:

[0005] To realize the above object, in accordance with the present invention, an electronic high frequency supply, such as a lamp ballast, having a double rectifier, two storage capacitors in series, and an isolating inductor between the rectifier and an AC input is provided. Each storage capacitor is charged to a voltage greater than the peak of the AC input. An inverter is connected to the storage capacitors, and has a high frequency inductive load circuit connected between an inverter output and a junction between the isolating inductor and the double rectifier. A capacitor, connected from the junction to the junction of two storage capacitors, forms a high frequency resonance circuit with the inductive load circuit. Current is drawn from the input AC only as a series of pulses at the inverter frequency. The isolating inductor filters out the high frequency part of the current pulse and makes the input current near sine wave.

Pages 4-5, amend paragraph [0021] as:

[0021] During a first stage of each high frequency cycle, immediately after transistor Q1 is switched on, because of the substantial inductance of inductor L1, current is still flowing in a direction from node N1 to node N3. The transistor Q2 ~~, being~~ is switched off, and current during this stage will flow in the "backwards" direction, through ~~though~~ freewheel diode D5 in a direction to charge C3, and through input power line (or filter) and coupling capacitor C7. The absolute value of the inductor current now falls rapidly. Voltage Vc2 across C2 drops until it goes to second stage. If this voltage drops below the voltage Vc4 across C4, it will be limited by D2 to voltage C4. The voltage drop is determined by power line input voltage, L1 current, L3, C1, L1, C8 and effective lamp resistance. Vc2-min, the envelop of the lowest level of the voltage drop is shown on

Figure 4. It is a half cycle of a sine wave with amplitude from –Vc4 to a certain voltage below the peak power line input voltage. This certain voltage is determined by the voltage drop on L3 at peak power line input.

Page 6, amend paragraph [0024] as:

[0024] When Vc2 reaches Vc2-min, the sixth stage is reached. The inductor current then flows through transistor Q2, storage capacitor C4 and the line or line filter, and through isolating inductor L3 and coupling capacitor C7. Immediately after the inverter again switches, and Q2 is turned off, this current will start to fall sharply as it flows through D5, in a charging direction through C3, through input power line (or filter) and coupling capacitor C7, thus repeating stage 1 as described above.

Page 6, amend paragraph [0025] as:

[0025] The six different stages of one high frequency cycle are only partly symmetrical. The storage capacitor C3 receives charging current during the first stage, and storage capacitor C4 may receive charging current during the fourth stage depending on the voltage drop, immediately following each switching of the inverter. C3 discharges during stage 2 when the voltage across C2 is being raised from Vc2-min to the value where diode D1 conducts. And C4 may charge during stage 6 when the voltage on C2 falls below –Vc4, which normally occurs when the power line voltage varies across 0.

Pages 6-7, amend paragraph [0027] as:

[0027] The average voltage across C2 reflects the average current through L1. When the component values and inverter frequency have been properly selected, the average

current through L3 [[match]] matches the power line input voltage waveform. Except for the high frequency pulsation, which is filtered by the interference filter, to the power line input, the ballast load looks like a pure resistance. Analysis shows that this requires that the value of storage capacitor C3 and C4 be sufficiently high so that Vc3 and Vc4 do not change appreciably over the course of a line voltage cycle, and requires that the voltage across C3 and C4 exceed the peak voltage of line input.